Refine Search

Search Results -

Terms	Documents
L12 same L3	7

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Search History

DATE: Friday, November 26, 2004 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
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L13	L12 same l3	7	L13
L12	L11 same l5	75	L12
L11	L10 same l1	75	L11
L10	super adj1 voltage	178	L10
L9	supper adj1 voltage	0	L9
L8	L7 same l1	36	L8
L7	L6 same l2	18786	L7
L6	L5 near3 l3	148503	L6
L5	voltage or potential	2371305	L5
L4	reference adj2 (voltage or potential)	189211	L4
L3	compar$	2623159	L3
L2	control near3 circuit	816999	L2
L1	test adj1 mode	18531	L1

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First Hit Previous Doc Next Doc Go to Doc#

End of Result Set

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L13: Entry 7 of 7 File: DWPI May 6, 1997

DERWENT-ACC-NO: 1997-271451
DERWENT-WEEK: 199724

TITLE: Super voltage detection circuit for IC test mode selection during burn-in - has FET operating as comparator receiving super voltage selectively at source which is also coupled to reference, with drain coupled to ground via resistance and indicating presence of super voltage at input

Standard Title Terms (1):
SUPER VOLTAGE DETECT CIRCUIT IC TEST MODE SELECT BURN FET OPERATE COMPARATOR RECEIVE SUPER VOLTAGE SELECT SOURCE COUPLE REFERENCE DRAIN COUPLE GROUND RESISTANCE INDICATE PRESENCE SUPER VOLTAGE INPUT

Previous Doc Next Doc Go to Doc#

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

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L8: Entry 8 of 36 File: USPT Nov 11, 2003

DOCUMENT-IDENTIFIER: US 6646936 B2

**** See image for Certificate of Correction ****

TITLE: Semiconductor memory device shiftable to test mode in module as well as semiconductor memory module using the same

Brief Summary Text (15):

For shifting DRAMs 631-648 to the test mode, test mode circuit 700 receives control signals CSA, CSB and CSC of H level, and also receives signal SVIH formed of a voltage level higher than the voltage level in a normal operating range. Thereby, N-channel MOS transistor 705 is turned on, and the differential circuit formed of P-channel MOS transistors 701 and 703 as well as N-channel MOS transistors 702 and 704 compares the voltage level of signal SVIH with the voltage level of reference voltage VDD, and sends the signal of L level from node 709 to inverter 711. Inverter 711 inverts this signal of L level, and outputs the signal of H level to AND gate 712. AND gate 712 performs a logical AND on the signal of H level sent from inverter 711 as well as control signals CSA and CSB of H level, and generates test mode signal TM of H level.

Detailed Description Text (179):

Differential comparing circuit 600 compares the voltage level of signal SVIH with the voltage level of reference voltage VDD, and outputs a signal of L level to inverter 611. Inverter 611 inverts the signal of L level to output a signal of H level to AND gate 612. AND gate 612 performs a logical AND on the signal of H level sent from inverter 611 and select signals SEL2 and SEL3 of H level which are externally supplied, and outputs test mode signal TM of H level to test content designating circuit 288 and control circuit 391.

Previous Doc Next Doc Go to Doc#

US006646936B2

(12) **United States Patent**
Hamamatsu et al.

(10) **Patent No.: US 6,646,936 B2**
(45) **Date of Patent: Nov. 11, 2003**

(54) **SEMICONDUCTOR MEMORY DEVICE SHIFTABLE TO TEST MODE IN MODULE AS WELL AS SEMICONDUCTOR MEMORY MODULE USING THE SAME**

(75) Inventors: **Akihito Hamamatsu**, Hyogo (JP); **Shinji Tanaka**, Hyogo (JP)

(73) Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/094,645**

(22) Filed: **Mar. 12, 2002**

(65) **Prior Publication Data**

US 2003/0035328 A1 Feb. 20, 2003

(30) **Foreign Application Priority Data**

Aug. 8, 2001 (JP) 2001-240686

(51) **Int. Cl.**[7] **G11C 7/00**

(52) **U.S. Cl.** **365/201**

(58) **Field of Search** 365/201, 189.09, 365/189.05, 189.11, 230.08, 233, 241, 225.7

(56) **References Cited**

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Primary Examiner—Thong Le
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) **ABSTRACT**

A DRAM includes a test mode circuit. Test mode circuit generates respective test mode signals of an L level and an H level by detecting first and second power supply voltages in response to first and second test mode shift signals, respectively. A control circuit controls peripheral circuits to input and output data for executing a special test to and from a plurality of memory cells in response to receiving of the test mode signals of an L level and an H level. Consequently, a semiconductor memory device can enter the test mode in a module.

20 Claims, 31 Drawing Sheets

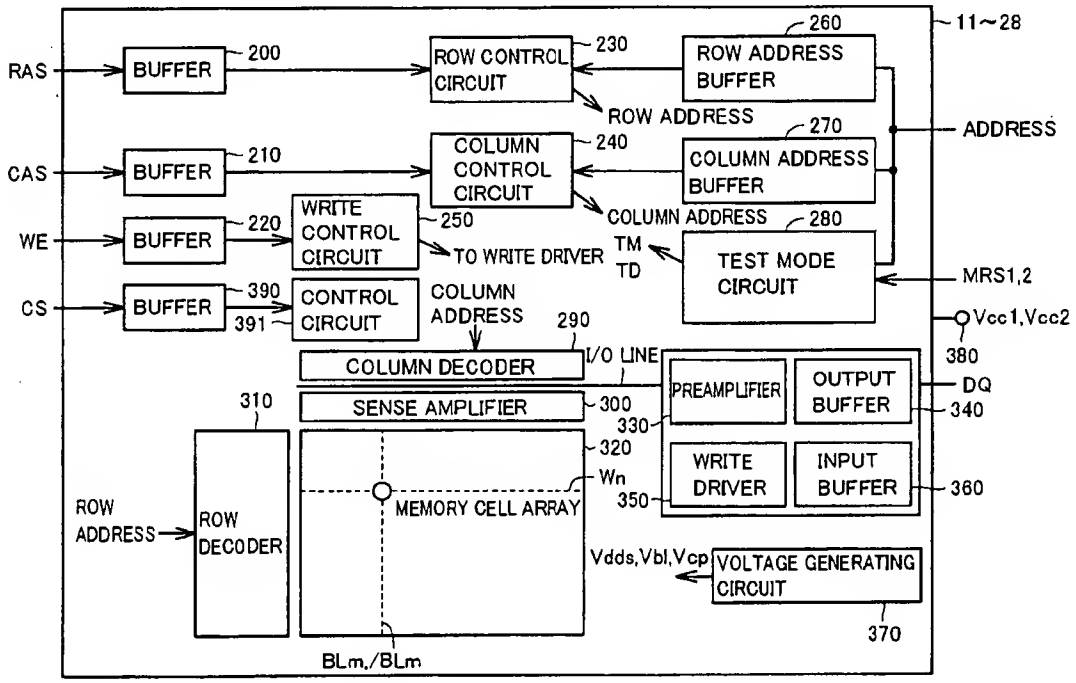
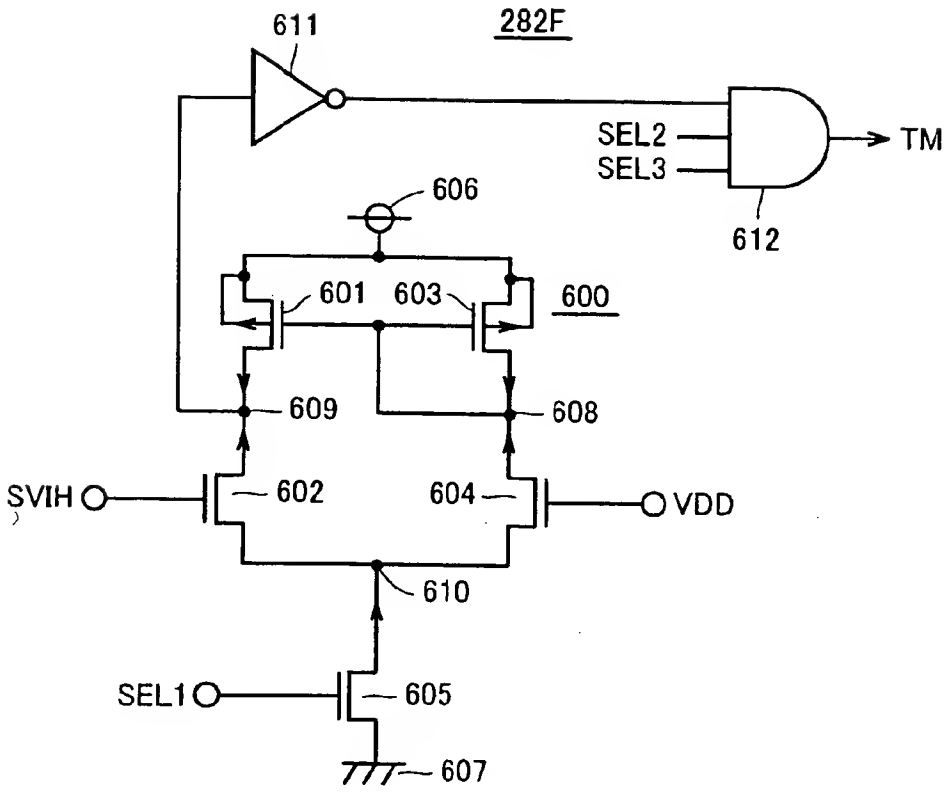


FIG.31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TM
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VDD
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US006550038B2

(12) **United States Patent**
Shirata

(10) **Patent No.: US 6,550,038 B2**
(45) **Date of Patent: Apr. 15, 2003**

(54) **SEMICONDUCTOR INTEGRATED CIRCUITRY**

(75) Inventor: **Shuuichi Shirata**, Tokyo (JP)

(73) Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 36 days.

(21) Appl. No.: **09/814,868**

(22) Filed: **Mar. 23, 2001**

(65) **Prior Publication Data**

US 2002/0046388 A1 Apr. 18, 2002

(30) **Foreign Application Priority Data**

Oct. 17, 2000 (JP) 2000-316684

(51) **Int. Cl.**[7] **G05F 1/56**

(52) **U.S. Cl.** **716/4**; 365/227; 324/537; 714/733

(58) **Field of Search** 716/4; 324/537, 324/763, 765, 713, 771; 365/226, 227; 714/30, 733, 734, 724

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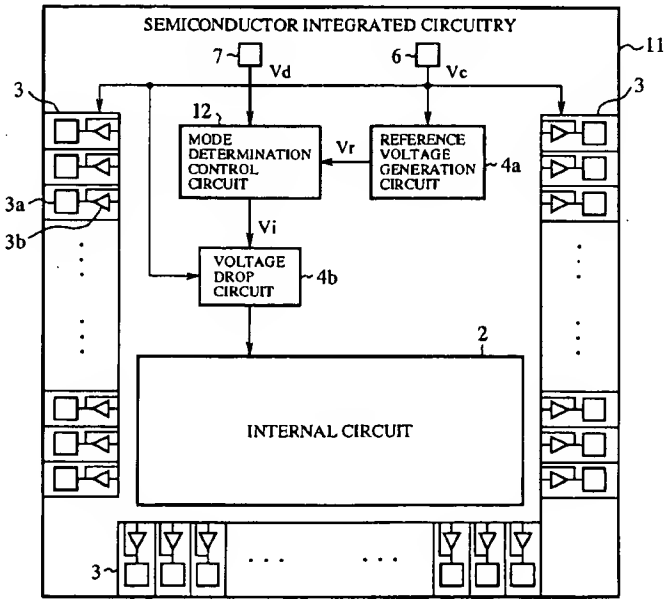
Primary Examiner—Tuan T. Lam
Assistant Examiner—Linh Nguyen
(74) *Attorney, Agent, or Firm*—Burns, Doane, Swecker & Mathis, LLP

(57) **ABSTRACT**

Semiconductor integrated circuitry comprises an I/O circuit for activating an input/output of an internal circuit in response to an external power supply voltage applied thereto, a reference voltage generation circuit for decreasing the external power supply voltage so as to generate a constant reference voltage, a voltage drop circuit for controlling the external power supply voltage so as to decrease it such that it is equal to an input voltage applied thereto, and for supplying the decreased external power supply voltage to the internal circuit, and a mode determination control circuit to which a power supply voltage for test is supplied from a power supply for test that is connected to a power supply terminal for test in test mode, for comparing the power supply voltage for test with a threshold voltage so as to determine whether the semiconductor integrated circuitry is placed in either normal operation mode or the test mode, and for supplying either the reference voltage or the power supply voltage for test to the voltage drop circuit as the input voltage according to the mode determination result.

6 Claims, 7 Drawing Sheets



L8: Entry 10 of 36 File: USPT Apr 15, 2003

DOCUMENT-IDENTIFIER: US 6550038 B2
TITLE: Semiconductor integrated circuitry

Abstract Text (1):
Semiconductor integrated circuitry comprises an I/O circuit for activating an input/output of an internal circuit in response to an external power supply voltage applied thereto, a reference voltage generation circuit for decreasing the external power supply voltage so as to generate a constant reference voltage, a voltage drop circuit for controlling the external power supply voltage so as to decrease it such that it is equal to an input voltage applied thereto, and for supplying the decreased external power supply voltage to the internal circuit, and a mode determination control circuit to which a power supply voltage for test is supplied from a power supply for test that is connected to a power supply terminal for test in test mode, for comparing the power supply voltage for test with a threshold voltage so as to determine whether the semiconductor integrated circuitry is placed in either normal operation mode or the test mode, and for supplying either the reference voltage or the power supply voltage for test to the voltage drop circuit as the input voltage according to the mode determination result.

Brief Summary Text (12):
In accordance with the present invention, there is provided semiconductor integrated circuitry comprising: an internal circuit that is an semiconductor integrated circuit; an I/O circuit for activating an input/output of the internal circuit in response to an external power supply voltage applied thereto; a reference voltage generation circuit for decreasing the external power supply voltage so as to generate a constant reference voltage; a voltage drop circuit for controlling the external power supply voltage so as to decrease it such that it is equal to an input voltage applied thereto, and for supplying the decreased external power supply voltage to the internal circuit; and a mode determination control circuit to which a power supply voltage for test is supplied from a power supply for test that is connected to a power supply terminal for test in test mode, for comparing the power supply voltage for test with a threshold voltage so as to determine whether the semiconductor integrated circuitry is placed in either normal operation mode or the test mode, and for supplying either the reference voltage or the power supply voltage for test to the voltage drop circuit as the input voltage according to the mode determination result.

CLAIMS:

1. Semiconductor integrated circuitry comprising: an internal circuit that is an semiconductor integrated circuit; an I/O circuit for activating an input/output of said internal circuit in response to an external power supply voltage applied thereto; a reference voltage generation circuit for decreasing said external power supply voltage so as to generate a constant reference voltage; a voltage drop circuit for controlling said external power supply voltage so as to decrease it such that it is equal to an input voltage applied thereto, and for supplying the decreased external power supply voltage to said internal circuit; and a mode determination control circuit to which a power supply voltage for test is supplied from a power supply for test that is connected to a power supply terminal for test in test mode, for comparing the power supply voltage for test with a threshold

voltage so as to determine whether said semiconductor integrated circuitry is placed in either normal operation mode or the test mode, and for supplying either the reference voltage or the power supply voltage for test to said voltage drop circuit as the input voltage according to the mode determination result.

Previous Doc Next Doc Go to Doc#

US005627485A

United States Patent [19]

Casper et al.

[11] Patent Number: 5,627,485

[45] Date of Patent: May 6, 1997

[54] **VOLTAGE-INDEPENDENT SUPER VOLTAGE DETECTION CIRCUIT**

[75] Inventors: **Stephen L. Casper; James E. Miller.** both of Boise, Id.

[73] Assignee: **Micron Technology, Inc.. Boise. Id.**

[21] Appl. No.: **494,483**

[22] Filed: **Jun. 26, 1995**

[51] **Int. Cl.**[6] **H03K 5/153**

[52] **U.S. Cl.** **327/77**; 327/78; 327/80; 327/530

[58] **Field of Search** 327/77, 78, 79, 327/80, 81, 74, 143, 142, 198, 530

[56] **References Cited**

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Prior Circuit used by Micron Technology, Inc. no date.

Primary Examiner—Toan Tran

Attorney, Agent, or Firm—Angus C. Fox, III

[57] **ABSTRACT**

This invention is a super voltage detection circuit that functions independent of power supply voltage. The circuit employs a reference node that is coupled to V_{CC} through a current-limiting device. The node is also coupled to ground via a plurality of series-coupled N-channel diodes. The current-sinking capability of the series-coupled diode path is greater than the current passing capability of the current-limiting device. Thus, a reference voltage is established at the node. The reference voltage is applied to the gate of a P-channel field-effect transistor which acts as a comparator device. The source region of the comparator device is coupled to an input terminal through a plurality of series coupled N-channel diodes. A super voltage may be selectively applied to the terminal. The source of the comparator device is also coupled to the reference node through an N-channel diode, which assures that the comparator transistor is always at a voltage lower than the gate when no super voltage is applied to the input terminal. The drain region of the comparator device is coupled to ground through a device which functions as a resistor. The voltage step-down between the input terminal and the source is set so that when a super voltage is applied to the terminal, the potential on the source rises above the gate voltage, thus initiating current flow through the comparator device. Therefore, the potential at the drain is indicative of the presence of a super voltage at the input terminal.

23 Claims, 1 Drawing Sheet